REMARKS

Present Status of the Application

The Office Action rejected presently-pending claims 1-19. Specifically, the Office Action rejected claims 1, 5-6, and 12-14 under 35 U.S.C. 102(b), as being anticipated by Akram et al. (U. S. Patent 5,994,166). In addition, the Office Action rejected claims 2-4 under 35 U.S.C. 103(a) as being unpatentable over Akram et al. in view of Higgins, III (U. S. Patent 6,064,114). The Office Action also rejected claims 7-11 and 15-19 under 35 U.S.C. 103(a) as being unpatentable over Akram et al. Applicants have amended independent claims 1 and 12 to only improve clarity without reducing the scope. Claims 1-19 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Office Action Rejections

The Office Action rejected claims 1, 5-6, and 12-14 under 35 U.S.C. 102(b), as being anticipated by Akram et al.. In addition, the Office Action rejected claims 2-4 under 35 U. S. C. 103(a) as being unpatentable over Akram et al. in view of Higgins, III. The Office Action rejected claims 7-11 and 15-19 under 35 U. S. C. 103(a) as being unpatentable over Akram et al.. Applicants respectfully traverse the rejections for at least the reasons set forth below.

The present invention is directed to a DCA memory module. The features are recited in independent claims 1 as follows:

1. A DCA memory module, comprising:
a substrate of a memory module;
at least a chip set ***having a plurality of chips formed side by side with each other***, wherein the chips are adhered on the substrate and are electrically connected to the substrate, ***a plurality of circuits not within the substrate are located between the chips and electrically connect the chips to each other***; and
a molding compound, encapsulating a portion of the electrical connection between the chip set and the substrate (*Emphasis added*).

Likewise, independent claim 12 recites:

12. A DCA memory module, comprising:
a substrate of a memory module;
at least a chip set, for adhering onto the substrate and electrically connecting to the substrate, wherein ***the chip set has a plurality of chips formed side by side as one group, wherein the chip set further includes a circuit to coupled the chips together***; and
a molding compound, for encapsulating a portion of the electrical connection between the chip set and the substrate (*Emphasis added*).

The features emphasized in claims 1 and 12 are at least not disclosed by the prior art references. In the present invention (i.e. in FIGs. 3-5), the chip set 250 has multiple chips 220 disposed side by side. The chips 220 are coupled together by a circuit, for example, in the metal layer 232, which is within the chip set ***but not within the substrate 260***. Therefore multiple chips are coupled side by side to form the chip set. Then chips or the chip set are adhered on the substrate. As a result (i.e. page 9, lines 13-17), the layout of the substrate of the memory module is simplified.

In the present invention, the chip set includes multiple chips disposed side by side, and the chips are coupled together by the circuit not within the substrate. These features as recited in claims 1 and 12 are at least not disclosed.

With respect to claims 1, 5-6, and 12-14, Akram et al. is cited for rejections under 35 U.S.C. 102 by the Office Action.

However, in re Akram et al. (see Fig. 1; col. 5, lines 65-67; col. 6, lines 1-12), the substrate 116 is a stacked substrate but not the base substrate 102. The stacked substrate is used for staking the chips but not the substrate of the memory module in the present invention.

Also and, Akram et al. failed to disclose the chips set of the present invention as recited in claims 1 and 12. Clearly, the semiconductor dice 128 are separately disposed on the stacked substrate 116, and then coupled to the base substrate 102 through the connections 126.

For at least the foregoing reasons, Akram et al. failed to disclose the features of the present inventions.

With respect to claims 7-11 and 15-19, since the chip set includes the circuit to couple multiple chips, the number of chips can vary as the choice. With at least the same foregoing reasons, Akram et al. treats the chips individually, even though a stacked structure is disclosed.

With respect to claims 2-4, the substrate is further defined. The Office Action cites Higgins, III (hereinafter Higgins)in combination with Akram et al. However, Higgins failed to disclose the missing features in Akram et al., as discussed above.

In re Higgins, each chip 10 is individually adhered on the substrate 50 (Figs. 1-3). No chip set has been disclosed.

Therefore, the claimed invention recited in claims 1 and 12 is distinguishable over Akram et al. and Higgins either alone or in combination.

For at least the foregoing reasons, Applicant respectfully submits that independent claims 1 and 12 patently define over the prior art0, and should be allowed. For at least the same reasons, dependent claims 2-11 and 13-19 patently define over the prior art as well.

CONCLUSION

For at least the foregoing reasons, it is believed that all pending claims 1-19 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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